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EXAMINER
VITAL, PIERRE M

ART UNIT	PAPER NUMBER
2188	2

DATE MAILED: 07/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/056,293	MEKKITTIKUL ET AL.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This Office Action is in response to Application No. 10/056,293 filed January 23, 2002. Claims 1-20 are pending in this application.

2. The specification and the claims have been examined with the results that follow.

Drawings

3. The drawings are objected to because of the following informalities:

The drawings are objected to under 37 CFR 1.83(a) because they fail to show a labeled representation of elements 201-203 in Fig. 2 as described in the specification. These elements are shown as empty box and it is not clear what they represent in the drawings. All drawings elements must be labeled in the manner of element 204 in the Figure. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). In this case, please label elements 201-203 with the term "packets" or "data packets" in Fig. 2.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

> All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the manner of a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings and **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

Claim Objections

4. Claims 1-3, 5, 8, 12-13 and 20 are objected to because of the following informalities:

(a) In claim 1, line 5, after "in parallel;", please insert --and--.

(b) In claims 2 and 3, after "comprising", please delete "the step of".

(c) In claims 5 and 20, it appears that "comprise" should be replaced with –comprises--.

(d) In claim 5, it appears that "Claim 1" should be replaced with –Claim 4--, since only claim 4 mentions the use of DRAM memory.

(e) In claim 8, line 2, after "in parallel;", please insert --and--.

(f) In claim 12, line 1, before "Claim 8", please delete –Claim element of--.

(g) In claim 13, line 2, after "memories", please insert --and--.

(h) In claim 20, it is not clear what "x" represents in the claim. Examiner would suggest amending the claim to indicate the relationship of "x" to "n" (*i.e.*, $x < n$, *etc.*) and whether "x" and "n" represent integer values.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 8, 11, 13-14, 17 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Chan et al. (US5,822,772).

As per claim 8, Chan discloses an apparatus comprising a plurality of memories coupled in parallel [*each command queue corresponds to a bank and is coupled in parallel with another bank, as shown in the figure*; Fig. 4; col. 5, lines 53-54]; a scheduler coupled to said plurality of memories [*Selection Logic 131*; Fig. 4], wherein the scheduler randomly selects which of said memories data is to be written [*each command queue corresponds to a row or bank of memory and selection of the queue is arbitrary, thus selection of the row or bank must also be arbitrary*; col. 5, lines 31-33, 49-61 and col. 7, lines 5-8].

As per claim 11, Chan discloses said plurality of memories comprise DRAM memory modules [*DRAM banks (i.e., several memory chips connected together to form a memory module)*; Fig. 2; col. 5, lines 40-42].

As per claim 13, Chan discloses an apparatus comprising a plurality of memories [*memory controller coupled to command queues, each command queue corresponds to a bank*; Fig. 4; col. 5, lines 49-54]; a memory controller coupled to said plurality of memories [*Selection*

Logic 131; Fig. 4], wherein data is written to random locations of said plurality of memories [*each command queue corresponds to a row or bank of memory and selection of the queue is arbitrary, thus selection of the row or bank must also be arbitrary*; col. 5, lines 31-33, 49-61 and col. 7, lines 5-8].

As per claim 14, Chan discloses the plurality of memories are coupled in parallel [*each command queue corresponds to a bank and are coupled in parallel as shown in the figure*; Fig. 4; col. 5, lines 53-54]; and total memory bandwidth equals a sum of memory bandwidths of said plurality of memories [*data in and from each bank is 8-bit and the data from the 4 banks is concatenated into or cascaded from a 32-bit word*; col. 2, lines 21-26].

As per claim 17, Chan discloses worst-case memory access latency is minimized [col. 3, lines 62-67].

As per claim 19, Chan discloses a probability that a memory is selected to read/write a packet into is randomly uniformly distributed [*data in and from each bank is 8-bit and the data from the 4 banks is concatenated into or cascaded from a uniformed 32-bit word*; col. 2, lines 21-26; *selection of the queue is arbitrary, thus selection of the row or bank must also be arbitrary*; col. 5, lines 49-61 and col. 7, lines 5-8].

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 9 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (US5,822,772) and Vogley (US6,260,106).

As per claim 9, Chan discloses the claimed invention as detailed above in the previous paragraphs. Chan further discloses a plurality of queues coupled to the plurality of memories [*each command queue corresponds to a row or bank of memory;* col. 5, lines 30-33], wherein said scheduler directs data to one of said plurality of queues randomly [*selection of the queue is arbitrary, thus selection of the row or bank must also be arbitrary*; col. 5, lines 49-61 and col. 7, lines 5-8].

However, Chan does not specifically teach the use of data packets as recited in the claim.

As one of ordinary skill in the art would transfer data to memory in a plurality of formats such as word, lines, packets or blocks, Vogley discloses the use of data packet as data being transferred [col. 1, lines 27-38].

It would have been obvious to one of ordinary skill in the art, having the teachings of Chan and Vogley before him at the time the invention was made, to modify the system of Chan to include the use of data packet as data being transferred because

it would have improved the data bandwidth of the system because with the appropriate use of address command and data packets the amount of time a data bus is idle can be minimized [col. 1, lines 35-38] as taught by Vogley.

As per claim 15, Chan discloses the claimed invention as detailed above in the previous paragraphs. Chan further discloses data are queued and stored in randomly selected memory modules of said plurality of memories [*selection of the queue is arbitrary, thus selection of the row or bank (i.e., module) must also be arbitrary*; col. 5, lines 49-61 and col. 7, lines 5-8].

However, Chan does not specifically teach the use of packets from a network as recited in the claim.

Vogley discloses the use of packets from a network as data being transferred [*Vogley discloses network nodes since packets are unit of information transferred as a whole from one device to another on a network*; col. 4, lines 30-31; col. 1, lines 27-38].

It would have been obvious to one of ordinary skill in the art, having the teachings of Chan and Vogley before him at the time the invention was made, to modify the system of Chan to include the use of packets from a network as data being transferred because it would have improved the data bandwidth of the system because with the appropriate use of command and address packets the amount of time a data bus is idle can be minimized [col. 1, lines 35-38] as taught by Vogley.

As per claim 16, Chan discloses said plurality of memory modules comprise DRAM memories [*DRAM banks (i.e., several memory chips connected together to form a memory module)*; Fig. 2; col. 5, lines 40-42].

9. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogley (US6,260,106) and Chan et al. (US5,822,772).

As per claim 1, Vogley discloses in a computer network having a plurality of network nodes, a method of buffering packets [*Vogley discloses network nodes since packets are unit of information transferred as a whole from one device to another on a network*; col. 4, lines 30-31], comprising receiving a packet incoming from said network [*FLAG signal indicates the beginning of the transmission of a packet*; Fig. 5; col. 5, lines 7-10]; storing said packet in said particular memory module [*command address bus indicates what type of operation is to be performed at which addresses within that storage module 500*; Fig. 5; col. 5, lines 10-16].

Even though Vogley further discloses that a plurality of memory modules coupled in parallel [*data storage module 500 include a number of packet based memory devices arranged in parallel*; Fig. 5; col. 6, lines 35-37]; Vogley does not specifically teach randomly selecting a particular memory module from a plurality of memory modules as recited in the claim.

Chan discloses randomly selecting a particular memory module from a plurality of memory modules [*each command queue corresponds to a row or bank of memory and selection of*

the queue is arbitrary, thus selection of the row or bank must also be arbitrary; col. 5, lines 31-33, 49-61 and col. 7, lines 5-8].

It would have been obvious to one of ordinary skill in the art, having the teachings of Vogley and Chan before him at the time the invention was made, to modify the system of Vogley to include randomly selecting a particular memory module from a plurality of memory modules because it would have (1) maximized the overall memory utilization efficiency and (2) minimized average memory access latency by eliminating penalties associated with row miss and/or page miss [col. 3, lines 62-67] as taught by Chan.

As per claim 2, Vogley discloses the claimed invention as detailed above in the previous paragraphs. However, Vogley fails to specifically teach queuing said packet in a queue corresponding to the particular memory module as recited in the claim.

Chan discloses queuing said packet in a queue corresponding to the particular memory module [*each command queue corresponds to a row and an incoming memory access command is dispatched to one of the command queues according to which memory row that this command is accessing*; Fig. 4, col. 5, lines 30-33, 55-61].

It would have been obvious to one of ordinary skill in the art, having the teachings of Vogley and Chan before him at the time the invention was made, to modify the system of Vogley to include queuing said packet in a queue corresponding to the particular memory module because it would have (1) maximized the overall memory utilization efficiency and (2) minimized average memory access latency by eliminating

penalties associated with row miss and/or page miss [col. 3, lines 62-67] as taught by Chan.

As per claim 3, Vogley discloses the claimed invention as detailed above in the previous paragraphs. However, Vogley fails to specifically teach reading data from said plurality of memory modules in a random order by which said data was written to said plurality of memory modules as recited in the claim.

Chan discloses reading data from said plurality of memory modules in a random order by which said data was written to said plurality of memory modules [*commands are completed our of order and selection of queues is arbitrary*; col. 6, line 62 – col. 7, line 30].

It would have been obvious to one of ordinary skill in the art, having the teachings of Vogley and Chan before him at the time the invention was made, to modify the system of Vogley to include reading data from said plurality of memory modules in a random order by which said data was written to said plurality of memory modules because it would have (1) maximized the overall memory utilization efficiency and (2) minimized average memory access latency by eliminating penalties associated with row miss and/or page miss [col. 3, lines 62-67] as taught by Chan.

As per claim 4, Vogley discloses said memory modules comprise DRAM modules [col. 1, lines 59-63].

10. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vogley (US6,260,106) and Chan et al. (US5,822,772) and further in view of Mathur (US6,424,658).

As per claim 5, the combination of Vogley and Chan discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Vogley and Chan does not specifically teach the use of a DRAM memory comprising 5Gbps bandwidth as recited in the claim.

Although Mathur does not specifically disclose that the DRAM memory comprises 5Gps bandwidth, the reference discloses the use of a DRAM memory producing a bandwidth in excess of 3Gbps [col. 5, lines 35-36]. Since applicant's invention and Mathur's system are directed to increasing memory depth or bandwidth of DRAM memories, claim 5 does not define a patentably distinct invention over that of Mathur and would have been obvious over the system of Mathur. The bandwidth of the DRAM as a whole presents no new or unexpected result so long as the DRAM's depth is large enough to store larger packets and allows transfer of the packets to one or more ports of a network switch [see Mathur, col. 6, lines 1-2]. Therefore, to have DRAM memory comprising 5Gps bandwidth in Mathur would have been obvious to one of ordinary skill in the art because it would have (1) increased the available memory depth, (2) minimize network overhead and (3) increased performance) by allowing large packets to be transmitted for many ports in the larger DRAM memory [col. 5, lines 40-45] as taught by Mathur.

11. Claims 6 and 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vogley (US6,260,106) and Chan et al. (US5,822,772).

As per claim 6, the combination of Vogley and Chan discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Vogley and Chan does not specifically teach the use of SRAM as the plurality of memories as recited in the claim.

The use of SRAM as a plurality of memories does not define a patentably distinct feature and is well known in the state of the art.

It would have been obvious to one of ordinary skill in the art, having the teachings of Vogley and Chan before him at the time the invention was made, to modify the system of Vogley and Chan to include the use of SRAM as the plurality of memories because it would have allowed the system to attain low power consumption by (1) providing a low consumption level of electric current in standby state and (2) providing working current for the refreshing operation having 10 or greater times less than the DRAM.

As per claim 7, the combination of Vogley and Chan discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Vogley and Chan does not specifically teach delays corresponding to writing data into said plurality of memory modules can be described by a binomial distribution as recited in the claim.

The use of a binomial (or Bernoulli) distribution to describe parameters in a system does not define a patentably distinct feature and is well known in the state of the art.

It would have been obvious to one of ordinary skill in the art, having the teachings of Vogley and Chan before him at the time the invention was made, to modify the system of Vogley and Chan to include delays corresponding to writing data into said plurality of memory modules that can be described by a binomial distribution because it would have allowed evaluation of the system performance by (1) comparing numerical results with results from simulation and (2) predicted potential error resulting from device utilization being estimated by sampling, rather than being measured directly.

12. Claims 10, 12, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (US5,822,772).

As per claims 10, 18 and 20, Chan discloses the claimed invention as detailed above in the previous paragraphs. However, Chan does not specifically teach delay associated with writing data to the plurality of memories can be described by a binomial distribution; that worst-case memory access latency is controlled by a binomial distribution; and that a probability that at least x of n requests will be written to a module comprise a binomial distribution function as recited in the claims.

The use of a binomial (or Bernoulli) distribution to describe parameters in a system does not define a patentably distinct feature and is well known in the state of the art.

It would have been obvious to one of ordinary skill in the art, having the teachings of Chan before him at the time the invention was made, to modify the system of Chan to include delays corresponding to writing data into said plurality of memory modules that can be described by a binomial distribution because it would have allowed evaluation of the system performance by (1) comparing numerical results with results from simulation and (2) predicted potential error resulting from device utilization being estimated by sampling, rather than being measured directly.

As per claim 12, Chan discloses the claimed invention as detailed above in the previous paragraphs. However, Chan does not specifically teach the use of SRAM as the plurality of memories as recited in the claim.

The use of SRAM as a plurality of memories does not define a patentably distinct feature and is well known in the state of the art.

It would have been obvious to one of ordinary skill in the art, having the teachings of Chan before him at the time the invention was made, to modify the system of Chan to include the use of SRAM as the plurality of memories because it would have allowed the system to attain low power consumption by (1) providing a low consumption level of electric current in standby state and (2) providing working current for the refreshing operation having 10 or greater times less than the DRAM.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach storing packets in randomly selected memory module and using binomial distribution to evaluate system parameters.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9000.

Pierre M. Vital
July 17, 2003